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Preparation of Semi-Insulating Silicon Carbide by Vanadium Doping During PVT Bulk Crystal Growth

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Although the use of vanadium doping to obtain semi-insulating (SI) SiC is well known and has been evaluated several times in the past [1], important issues limit both yield and electrical properties of semi-insulating wafers cut from vanadium-doped PVT-grown crystals. They will be addressed in the presentation as follows.

When added as a solid source to the SiC starting material, vanadium will deplete during growth, leading to inhomogeneous incorporation. We will show that depletion can be avoided by lowering the growth temperature and using an inner container filled with a SiC/VC-mixture. This leads to homogeneous vanadium incorporation in the crystals, resulting in homogeneous electrical properties. At room temperature, specific resistivities ρ in the range of 10^{11} Ωcm, charge carrier concentrations of 10^6 cm^{-3}, and mobilities around 30 cm^2/Vs with an overall electrical homogeneity of $\Delta\rho/\rho < 50\%$ are determined using the scanning capacitance method and extrapolation of temperature-dependent Hall effect measurements.

Due to the low solubility of vanadium in SiC of 5×10^{17} cm^{-3}, lowering the impurity incorporation during growth is crucial to obtain a high yield of semi-insulating material. We will discuss the effectiveness of a pre-heating step under high vacuum on the impurity incorporation which diminishes the nitrogen concentration in the crystals about one order of magnitude to below 5×10^{16} cm^{-3}. Additional measures to reduce further the impurity level in the crystals will be considered as reducing the total impurity amount is the key also for better substrate performance in device technology.

With nitrogen being the main impurity in the growth cell, only the vanadium acceptor level can be activated, while vanadium/boron co-doping facilitates the activation of the mid-gap vanadium donor level which leads to superior insulating properties as is shown in fig. 1. However, different time-dependent incorporation of many dopants, i.e. nitrogen, boron, and vanadium, has to be taken into account. Issues of co-doping technology, time-dependent compensation regimes and semi-insulating wafer yield will be addressed.

We have developed non-contact, non-destructive techniques to determine the semi-insulating behavior of vanadium doped SiC. Semi-insulating behavior can be determined at room temperature using optical absorption (see fig. 2), scanning capacitance and magnetic measurements, although some limitations occur in verifying the compensation mechanism, i.e. if the vanadium acceptor or the mid-gap vanadium donor level is active.

After all, vanadium doping is a promising approach for obtaining semi-insulating properties in silicon carbide bulk crystals, and it can be facilitated to prepare SI SiC wafers with homogeneous properties at high yield in a reproducible manner.

[1] W.C.Mitchel, R.Perrin, J.Goldstein, M.Roth, M.Ahoujja, S.R.Smith, A.O.Evwaraye, J.S.Solomon, G.Landis, J.Jenny, H.McD.Hobgood, G.Augustine, V.Balakrishna, Mater. Sci. Forum 264–268 (1998) 545

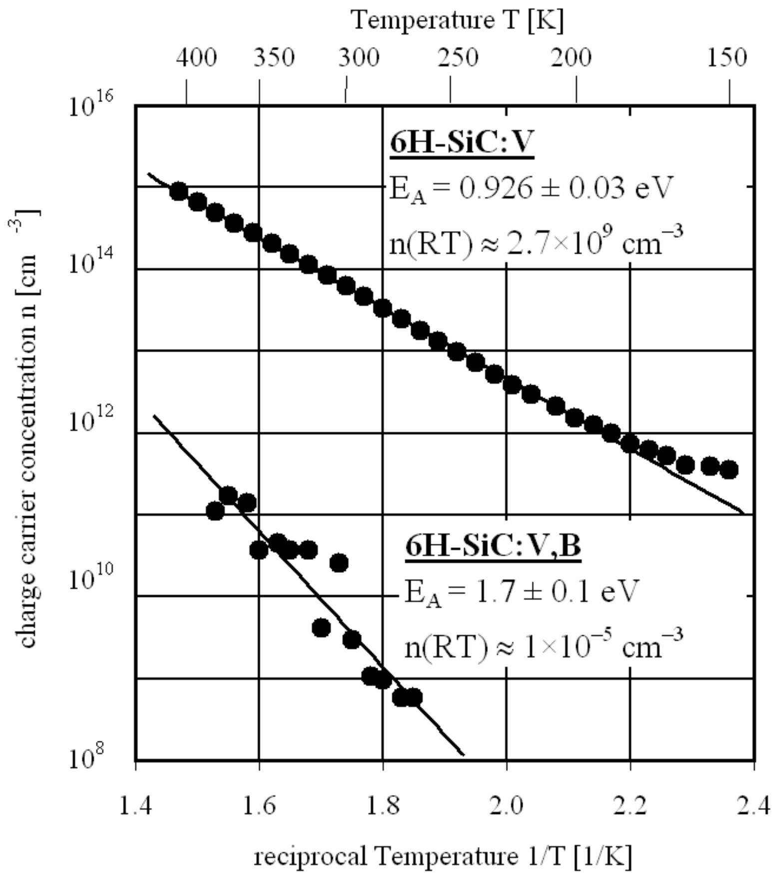

Fig. 1: Hall effect measurements of a V doped and a V,B co-doped 6H-SiC sample. Activation energies were determined using $\log(nT^{-1,5})=A-(E_A/kT)$ according to [1]. Charge carrier concentration n(RT) at 293 K is linearly extrapolated from the high temperature Hall effect data.

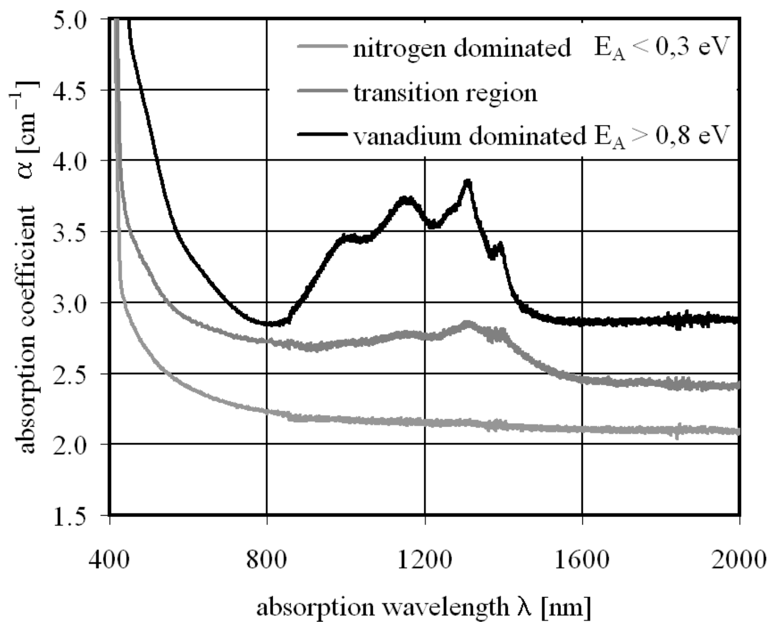

Fig. 2: The occurrence of V^{4+}-related absorption peaks in optical absorption at room temperature can be related to the electrical properties and thus reveals the predominant compensation mechanism in SiC:V and SiC:V,B samples.